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    (FILE 'USPAT' ENTERED AT 07:10:51 ON 07 AUG 95)
                     E (SUZUKI, MASATO)/IN
L1              29 S E3
L2           69948 S (395 OR 364 OR 371)/CLAS
L3               3 S L1 AND L2
                     E (KAMIYAMA, HIROSHI)/IN
L4               3 S E3
                     E (MIYAJI, SHINYA)/IN
L5               0 S 364/261.81/CLS
L6              95 S 364/262.81/CLS
L7             118 S 364/240.3/CLS
L8             209 S L6 OR L7
L9            8649 S (OVERFLOW? OR (OVER (W) FLOW?))/TI,AB,CLM
L10              1 S L8 AND L9
L11         716073 S EXTEN?/TI,AB,CLM
L12          45926 S COMPENSAT?/TI,AB,CLM
L13             22 S L8 AND L11
L14             17 S 4361868/UREF
L15              1 S L8 AND L12
L16            468 S (364/948.2 OR 364/948.21 OR 364/948.22)/CLS
L17              0 S L8 AND L16
                     SET HIGHLIGHTING ON
L18              0 S L14 AND L8
=> d l13 20 cit,ab
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20. 4,361,868, Nov. 30, 1982, Device for increasing the length of a logic computer address; Cecil H. Kaplinsky, 395/400; 364/232.8, 243, 246.6, 246.7, 248.1, 252, 254.9, 255.1, 255.5, 256.3, 259, 259.2, 262.4, **262.81**, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,361,868 [IMAGE AVAILABLE] L13: 20 of 22

ABSTRACT:
A data processing machine having a device for **extending** the length of the logic address to (M+N) bits, so that 2.sup.M+N different logic addresses can be formed and become available to the programmer. The original data structure of a computer having a word length of only N bits is then maintained. Programs written for the original machine can be executed without modification. A register bank of a data processing machine having its **extension** has a first section having a width of N bits which forms the least-significant side or tail, and a second section which has a width of M bits and which forms the more significant side or head. The first section is used in all instructions which utilize an operand from a register or which store an operand in a register, in the same manner as in the computer without the **extension**. The second section is used only if reference is made to the memory while using a register as a base register or as an index register; or if a special, new instruction is issued in order to load or store the content of the register thus addressed. The M additional address bits in the **extension** of the register provide the bits of higher significance in a physical or virtual address. Or they can also provide a segment number which is used in a subsequent conversion of the segmented virtual address into a physical address. In the segmented case, it is not necessary to apply a carry output signal from the section having a width of N bits to the section of the register having a width of M bits.

=> d l14 16 cit,ab

16. 4,453,212, Jun. 5, 1984, Extended address generating apparatus and

method; Blaine D. Gaither, et al., 395/400; 364/232.1, 238.4, 246, 246.3, 255.1, 255.2, 255.5, 256.3, 256.4, 256.5, 262.4, 262.8, 285, 285.3, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,453,212 [IMAGE AVAILABLE] L14: 16 of 17

ABSTRACT:
Address generating apparatus which uses narrow data paths for generating a wide logical address and which also provides for programs to access very large shared data structures outside their normally available addressing range and over an extended range of addresses. Selective indexed addressing is employed for providing index data which is also used for deriving variable dimension override data. During address generation, selected index data is added to a displacement provided by an instruction for deriving a dimension override value as well as an offset. The derived dimension override value is used to selectively access an address locating entry in a table of entries corresponding to the applicable program. The resulting accessed address locating entry is in turn used to determine the particular portion of memory against which the offset is to be applied.
=> d l14 cit 1-17

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2. 5,426,751, Jun. 20, 1995, Information processing apparatus with address extension function; Hideo Sawamoto, 395/400; 364/245.31, 255.1, 255.7, 256.3, 256.4, DIG.1 [IMAGE AVAILABLE]

3. 5,423,013, Jun. 6, 1995, System for addressing a very large memory with real or virtual addresses using address mode registers; Richard I. Baum, et al., 395/400; 364/DIG.1; 395/425 [IMAGE AVAILABLE]

4. 5,355,463, Oct. 11, 1994, Circuit configuration for transforming the logical address space of a processor unit to the physical address space of a memory; Udo Moeller, 395/400; 364/244.3, 247, 254.5, 255.1, 256.3, DIG.1; 395/375, 725 [IMAGE AVAILABLE]

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7. 5,136,699, Aug. 4, 1992, Logical address generating device for an instruction specifying two words, each divided into two parts; Yasushi Yokoyama, 395/400, 425 [IMAGE AVAILABLE]

8. 5,134,694, Jul. 28, 1992, Method and device for the processing of address words; Christian Jousselin, et al., 395/400; 364/927.97, 927.99, 933.2, 933.7, 942.04, 944.92, 947, 947.1, 947.3, 949, 955, 955.1, 955.2, 955.5, 955.6, 957.5, 958.3, 959, 961.1, 961.3, 963.2, 963.3, DIG.2 [IMAGE

AVAILABLE]

9. 5,023,777, Jun. 11, 1991, Information processing system using domain table address extension for address translation without software modification; Hideo Sawamoto, 395/400; 364/245, 245.31, 246, 246.3, 247, 247.5, 247.6, 247.8, 251, 251.3, 252.6, 254, 254.3, 255.1, 255.5, 255.7, 255.8, 256.3, 256.4, 260.6, 262.4, 955.6, 957.1, 958.3, 970.5, DIG.1 [IMAGE AVAILABLE]

10. 4,965,720, Oct. 23, 1990, Directed address generation for virtual-address data processors; Glen R. Mitchell, et al., 395/400; 364/228.2, 247, 247.2, 255.1, 255.7, 256.3, 256.4, DIG.1 [IMAGE AVAILABLE]

11. 4,807,119, Feb. 21, 1989, Memory address mapping mechanism; Masao Suga, 395/400; 364/231, 232.9, 234, 236.2, 237.2, 238.3, 243, 244, 244.6, 246, 246.3, 248.1, 252, 259, 259.9, DIG.1 [IMAGE AVAILABLE]

12. 4,796,177, Jan. 3, 1989, Address extension system; Hisayuki Nishimura, et al., 395/400; 364/247, 247.8, 255.1, 255.5, 258, 258.1, 259, 259.5, DIG.1 [IMAGE AVAILABLE]

13. 4,679,140, Jul. 7, 1987, Data processor with control of the significant bit lengths of general purpose registers; Shizuo Gotou, et al., 395/775; 364/DIG.1 [IMAGE AVAILABLE]

14. 4,677,548, Jun. 30, 1987, LSI microprocessor chip with backward pin compatibility and forward expandable functionality; John J. Bradley, 395/800; 364/968, 969.2, DIG.1 [IMAGE AVAILABLE]

15. 4,473,878, Sep. 25, 1984, Memory management unit; John E. Zolnowsky, et al., 395/400; 364/229, 229.2, 238.4, 244, 244.6, 246, 246.3, 247, 247.4, 247.8, 253, 253.1, 255.1, 255.5, 256.3, 256.5, 259, 259.2, 259.7, 263, DIG.1 [IMAGE AVAILABLE]

16. 4,453,212, Jun. 5, 1984, Extended address generating apparatus and method; Blaine D. Gaither, et al., 395/400; 364/232.1, 238.4, 246, 246.3, 255.1, 255.2, 255.5, 256.3, 256.4, 256.5, 262.4, 262.8, 285, 285.3, DIG.1 [IMAGE AVAILABLE]

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11. 4,635,192, Jan. 6, 1987, Self configuring bus structure for computer network; Claude R. Ceccon, et al., 395/325; 361/683; 364/228, 228.5, 229, 229.2, 232.2, 232.7, 232.9, 238.2, 240, 240.1, 240.2, **240.3**, 240.5, 242.94, 242.96, 244, 244.3, 263.3, 280.2, 284, 284.3, DIG.1 [IMAGE AVAILABLE]

12. 4,597,041, Jun. 24, 1986, Method and apparatus for enhancing the operation of a data processing system; James M. Guyer, et al., 395/375; 364/228.3, 238, 238.4, 239, 239.3, 244, 244.6, 246.91, 259, 259.5, 262.4, 262.8, **262.81**, 263.1, 280, 280.9, DIG.1 [IMAGE AVAILABLE]

13. 4,519,034, May 21, 1985, I/O Bus clock; Gehrard J. Smith, et al., 395/550; 364/228.3, 228.5, 229, 229.2, 234, 236.2, 236.3, 238.3, 238.4, 238.5, 240, 240.2, **240.3**, 240.5, 241.9, 243, 243.4, 243.41, 248.1, 248.2, 270, 271, DIG.1 [IMAGE AVAILABLE]

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Morrison, 395/425; 364/240, 246.4, 252, 252.6, 254.9, **262.81**, 263, 715.08, 736.5, DIG.1 [IMAGE AVAILABLE]

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17. 4,449,184, May 15, 1984, **Extended** address, single and multiple bit microprocessor; William Pohlman, III, et al., 395/250; 364/232.9, 232.93, 238, 239, 239.7, 239.9, 240, 240.1, **240.3**, 240.7, 241.2, 241.6, 244, 244.3, 244.6, 245, 245.4, 247, 247.2, 251, 251.3, 251.4, 252.3, 252.6, 255.1, 255.3, 255.8, 258, 258.4, 261.3, 261.5, 262.4, 262.8, 263.1, 270, 270.4, 270.5, 270.7, 271.6, 271.8, DIG.1; 395/275 [IMAGE AVAILABLE]

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19. 4,363,091, Dec. 7, 1982, **Extended** address, single and multiple bit microprocessor; William B. Pohlman, III, et al., 395/400; 364/232.8, 243, 244, 244.3, 244.6, 245, 245.1, 245.31, 254.8, 254.9, 258, 258.2, 258.3, 259, 259.2, 262.4, **262.81**, 262.9, 263, 263.1, DIG.1 [IMAGE AVAILABLE]

20. 4,361,868, Nov. 30, 1982, Device for increasing the length of a logic computer address; Cecil H. Kaplinsky, 395/400; 364/232.8, 243, 246.6, 246.7, 248.1, 252, 254.9, 255.1, 255.5, 256.3, 259, 259.2, 262.4, **262.81**, DIG.1 [IMAGE AVAILABLE]

21. 4,293,907, Oct. 6, 1981, Data processing apparatus having op-code **extension** register; Victor K. Huang, et al., 395/375; 364/238, 240.1, 243, 244, 244.3, 244.6, 251, 251.1, 251.2, 252, 259, 259.5, 261, 261.1, 261.2, 262.4, **262.81**, DIG.1 [IMAGE AVAILABLE]

22. 4,258,419, Mar. 24, 1981, Data processing apparatus providing variable operand width operation; Donald E. Blahut, et al., 395/375; 364/232.8, 238, 240.1, 243, 244, 244.6, 251, 251.1, 252, 254.8, 254.9, 259, 259.2, 259.5, 261, 261.2, 262, **262.81**, DIG.1 [IMAGE AVAILABLE]

21. 4,293,907, Oct. 6, 1981, Data processing apparatus having op-code **extension** register; Victor K. Huang, et al., 395/375; 364/238, 240.1, 243, 244, 244.3, 244.6, 251, 251.1, 251.2, 252, 259, 259.5, 261, 261.1, 261.2, 262.4, **262.81**, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,293,907 [IMAGE AVAILABLE] L13: 21 of 22

ABSTRACT:
A Central Processing Unit (CPU) includes a hardware op-code **extending** register (OER) for storing a code for programmable selection of optional CPU features which modify processor operations defined by the op-code in each instruction. A control section in the CPU decodes both the op-code of a current instruction and the code in the OER, effectively combining the two to form an **extended** op-code capable of defining a larger set of processor operations than the op-code carried in each instruction. The code in the OER is changed only when the CPU executes an instruction for transferring a new code into OER. Thus the code in OER can remain stationary over many instruction cycles.

22. 4,258,419, Mar. 24, 1981, Data processing apparatus providing variable operand width operation; Donald E. Blahut, et al., 395/375; 364/232.8, 238, 240.1, 243, 244, 244.6, 251, 251.1, 252, 254.8, 254.9, 259, 259.2, 259.5, 261, 261.2, 262, **262.81**, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,258,419 [IMAGE AVAILABLE] L13: 22 of 22

ABSTRACT:
A Central Processing Unit provides programmable variation of the operand width for processor operations. The operands are formed with one or more N-bit segments. The CPU includes an arithmetic logic unit (ALU) which is adapted to operate serially on one N-bit segment of the operand at a time beginning with the least significant segment and repeating the operation on the remaining segments according to their order of significance. The number of repetitions of an ALU operation is controlled by a code stored in an op-code **extension** register (OER). The code in the OER can be changed by means of an instruction for transferring a new code to OER.